Patent Claims:

1. Method of improving the immunity to interference of an integrated circuit (16), wherein error signals are transferred between at least one microprocessor chip or multiple processor µC (1) and at least one further component (2) in the form of one or more error signals, c h a r a c t e r i z e d in that for the transfer, a minimum pulse length that is independent of the clock frequency of the microprocessor or the microprocessors is defined, starting from which a signal on an error line having a defined pulse length is interpreted as an error.

2. Method of improving the immunity to interference of an integrated circuit (16), wherein error signals are transferred between at least one microprocessor module or multiple processor module and at least one further mixed-signal module in the form of one or more error signals, with the said modules being integrated on a chip or in a chip housing,
c h a r a c t e r i z e d in that for the transfer, a minimum pulse length that is independent of the clock frequency of the microprocessor or the microprocessors is defined, starting from which a signal on an error line having a defined pulse length is interpreted as an error.

3. Method as claimed in claim 1 or 2,
c h a r a c t e r i z e d in that in the event of a sequence of errors with a distance between the errors

that is smaller than the minimum pulse length, the time of the sequence of errors output over the at least one error line is extended with respect to the actual error sequence time.

4. Method as claimed in at least any one of claims 1 to 3, c h a r a c t e r i z e d in that the error signal(s) in a chip, which receives the error signal(s) of another chip or component, are particularly not processed when the signals do not reach a minimum duration, and are particularly processed when the minimum duration is reached or exceeded, and to this end the signals are directed in particular through at least one filter, in particular a low-pass filter (7, 7').

5. Method as claimed in at least any one of the preceding claims,
c h a r a c t e r i z e d in that at least one watchdog time window (17) is predetermined in the integrated circuit or in the further component (2), within which at least one artificially produced error signal or error signal pattern is generated and tested so that the error detection circuits become self-testable.

6. Method as claimed in at least any one of the preceding claims,
c h a r a c t e r i z e d in that the watchdog time window (17) has a delay time $T_{WindowDelay}$, and the time window, in which at least one error signal or error signal pattern is expected, remains open until the

expiry of the delay time $T_{WindowDelay}$.

7. Method as claimed in claim 5,
c h a r a c t e r i z e d in that the delay time $T_{WindowDelay}$ is longer than the filter time T_{Filter} of the filter(s) (7, 7') processing the error signal or error signals of the at least one error line (3, 3').

8. Method as claimed in at least any one of the preceding claims,
c h a r a c t e r i z e d in that inside the chip (1) that sends error signals, the error signals are extended and/or output with delay one after the other through the error line(s).

9. Method as claimed in at least any one of the preceding claims,
c h a r a c t e r i z e d in that a test of the at least one error line (3, 4) is performed with the aid of the interface (5).

10. Method as claimed in at least any one of the preceding claims,
c h a r a c t e r i z e d in that the error signals are filtered by filters (7, 7') with a defined filter time T_{Filter}.

11. Method as claimed in at least any one of the preceding claims,
c h a r a c t e r i z e d in that the time window $T_{WindowDelay}$ is set in the further component (2) by way of the interface (5) connected to chip (1).

12. Method as claimed in at least any one of the preceding claims,
c h a r a c t e r i z e d in that the condition $T_{WindowDelay}$ is satisfied in excess of the filter time T_{Filter}.

13. Method as claimed in at least any one of the preceding claims,
c h a r a c t e r i z e d in that the delay $T_{WindowDelay}$ approximately corresponds to twice the time T_{Filter}.

14. Method as claimed in at least any one of the preceding claims,
c h a r a c t e r i z e d in that the pulse width T_{Min} is set to a value of at least 30 nanoseconds approximately.

15. Integrated circuit, in particular in such a fashion that the above method is implemented, comprising
- at least one microprocessor chip or multiple processor microcontroller (1) or microprocessor module and at least one additional separate component (2) or a mixed-signal module integrated in the same component and comprising in particular separately arranged power elements, and
- one or more pulse extending devices and/or signal delaying devices for the output of error pulses (6, 6') one after the other through at least one error line (3, 4).

16. Integrated circuit as claimed in claim 15, c h a r a c t e r i z e d by one or more filters (7, 7') for filtering the error signals transferred through the error lines (3, 4).

17. Integrated circuit, in particular in such a fashion that the method as claimed in any one of claims 1 to 14 is implemented, comprising
    - at least one microprocessor chip or multiple processor microcontroller (1) and at least one additional component (2) comprising in particular separately arranged power elements, and
    - one or more filters (7, 7') for filtering error pulses (6, 6') through at least one error line (3, 4).

18. Integrated circuit as claimed in at least any one of the preceding claims related to the circuit, c h a r a c t e r i z e d in that the filter (7, 7') is configured as a digital forward/backward counter.

19. Integrated circuit as claimed in at least any one of the preceding claims related to the circuit, c h a r a c t e r i z e d in that the chips or components are interconnected by at least one bus (5) and at least one error line (3, 4).

20. Integrated circuit as claimed in at least any one of the preceding claims related to the circuit, c h a r a c t e r i z e d in that the circuit comprises hardware test structures, with the aid of which a test of the at least one error line (3, 4) can

be performed using an interface (5).

21. Integrated circuit as claimed in at least any one of the preceding claims related to the circuit, c h a r a c t e r i z e d in that the microprocessor chip (1) or the additional component comprises at least one watchdog window circuit (50).

22. Integrated circuit as claimed in claim 21, c h a r a c t e r i z e d in that the watchdog window circuit (50) predefines a watchdog time window (17), and the watchdog time window (17) has a delay time $T_{WindowDelay}$, and the time window, in which at least one error signal or error signal pattern is expected, remains open until the expiry of the delay time $T_{WindowDelay}$.

23. Integrated circuit, in particular in such a fashion that the method as claimed in any one of claims 1 to 14 is implemented, comprising
- at least one microprocessor chip or multiple processor microcontroller (1) and at least one additional component (2) comprising in particular separately arranged power elements, and
- at least one watchdog-window circuit (5) which predefines a watchdog time window (17), and the watchdog time window (17) has a delay time $T_{WindowDelay}$, and the time window, in which at least one error signal or error signal pattern is expected, remains open until the expiry of the delay time $T_{WindowDelay}$.

24. Integrated circuit as claimed in at least any one of the preceding claims related to the circuit, c h a r a c t e r i z e d in that the delay time $T_{WindowDelay}$ is longer than the filter time T_{Filter} of the filter(s) (7, 7') processing the error signal(s) of the at least one error line (3, 3').